IN THE CLAIMS

Please Amend the Claims in accordance with the following mark-up copy:

1. (Currently Amended) A method for managing energy use in a multi-threaded processing system, said method comprising:

first measuring the per-thread usage of a device by each thread in a first set of multiple threads concurrently executing within said multi-threaded processing system, said measured usage comprising an indicator for each of said multiple threads, wherein said device is a device coupled to and external to a processor executing said first set of multiple threads;

storing said measured per-thread usage for each of said first set of threads;

determining a next set of threads scheduled for execution;

retrieving [[a]] previously-stored per-thread measured usage of said device ~~for~~ corresponding to said next set of threads;

predicting a usage of said device by said next set of threads in conformity with said retrieved usage; and

sending a power management command to said device in conformity with a result of said predicting ~~retrieving~~, whereby a power management state of said device is set in conformity with said previously-stored measured usage ~~for~~ corresponding to said next set of threads.

2. (Original) The method of Claim 1, further comprising setting a state of said first measuring for said next set of threads in conformity with a result of said retrieving and determining.

3. (Currently Amended) The method of Claim 1, further comprising:

setting a threshold level of total usage for said device in conformity with said retrieved previously-stored measured usage for said next set of threads;

second measuring a total usage of said device by all of said next set of threads; and

second determining whether or not said total usage has fallen below said threshold, and wherein said sending is performed in response to a result of said second determining.

4. (Original) The method of Claim 3, wherein said first measuring comprises collecting per-thread counts of accesses to said device in one or more performance monitor units, wherein said second measuring comprises counting total accesses to said device within a device controller coupled to said device, wherein said second determining is performed within said device controller, and wherein said sending is performed automatically in response to said second determining, whereby said power management state of said device is set automatically by said device controller without intervention by a processor of said processing system.

5. (Original) The method of Claim 1, wherein said device is a memory module, wherein said sending sends power management setting information to said memory module, wherein said first measuring determines a frequency of accesses to said memory module by each of multiple threads, and wherein said second measuring determines an overall frequency of access to said memory module by all of said next set of threads.

6. (Original) The method of Claim 1, wherein said first measuring comprises collecting per-thread counts of accesses to said device within a device controller coupled to said device, wherein said second measuring comprises counting total accesses to said device within said device controller, wherein said second determining is performed within said device controller, and wherein said sending is performed automatically in response to said second determining, whereby said power management state of said device is set automatically by said device controller without intervention by a processor of said processing system.

7. (Currently Amended) A multi-threaded processing system, comprising:

at least one processor core capable of simultaneous execution of multiple threads;

a memory coupled to said processor for storing program instructions and data values for each of said multiple threads;

a device controller coupled to said processor;

one or more controlled devices coupled to said device controller, wherein said controlled devices have multiple power management states; and

a per-thread usage monitor coupled to said device controller for determining a usage of said one or more controlled devices for each thread in a first set of threads concurrently executing within said multi-threaded processing system and further having an output port coupled to said at least one processor core, whereby said at least one processor core retrieves values of said per-thread usage monitor and stores said values in said memory at a context switch, wherein said at least one processor core retrieves previously stored per-thread device usage values ~~for~~ corresponding to a next set of threads scheduled for execution in a next execution slice and predicts a usage of said device by said next set of threads in conformity with said retrieved usage, wherein said device controller includes a command unit for sending commands to said one or more controlled devices, and wherein said command unit is controlled for said next execution slice in conformity with said predicted usage of said device by ~~said retrieved previously stored values for~~ said next set of threads.

8. (Original) The multi-threaded processing system of Claim 7, wherein said per-thread usage monitor further has an input port

coupled to said at least one processor core, whereby said processor core further sets an initial state of said per-thread usage monitor for said next execution slice in conformity with said retrieved previously stored values.

9. (Original) The multi-threaded processing system of Claim 7, wherein said device controller further comprises at least one total usage evaluator having an input coupled to an output of said command unit for evaluating a frequency of use of an associated controlled device, and control logic coupled to said usage evaluator and further coupled to an input of said command unit for sending power management commands in response to said usage evaluator detecting that a usage level of said associated device has fallen below a threshold level, whereby said device controller power manages said controlled device without intervention by said processor, and wherein said processor core programs said threshold level for said next execution slice in conformity with said retrieved previously stored values for said next set of threads.

10. (Original) The multi-threaded processing system of Claim 7, wherein said device controller is a memory controller, and wherein said controlled devices are memory modules.

11. (Original) The multi-threaded processing system of Claim 7, wherein said per-thread usage monitor is included within a performance monitor unit coupled to said device controller.

12. (Original) The multi-threaded processing system of Claim 7, wherein said per-thread usage monitor comprises a plurality of performance monitor units, each associated with a particular one of said multiple threads.

13. (Original) The multi-threaded processing system of Claim 7, wherein said per-thread usage monitor is included within said device controller.

14. (Original) The multi-threaded processing system of Claim 7, wherein said per-thread usage monitor comprises multiple sets of usage counters, each of said sets associated with one of multiple threads executing within said processing system and wherein each set comprises a usage counter for each of said controlled devices, whereby a usage count of each device for each thread is maintained.

15. (Currently Amended) A computer program product comprising signal-bearing media encoding program instructions for execution within a multi-threaded processing system, said program instructions comprising program instructions for:

first retrieving per-thread usage of a device from a hardware performance monitor that measures usage of said device by each thread in a first set of multiple threads concurrently executing within said multi-threaded processing system, said measured usage comprising an indicator for each of said multiple threads, and wherein said device is external to a processor executing said multiple threads and is coupled to said processor by a device controller;

storing said measured per-thread device usage for each of said first set of threads;

determining a next set of threads scheduled for execution;

second retrieving [[a]] previously-stored per-thread measured device usages ~~for~~ corresponding to said next set of threads;

predicting a usage of said device by said next set of threads in conformity with said retrieved usage; and

sending control information to [[a]] said device controller in conformity with a result of said predicting ~~retrieving~~, whereby a power management state of said device is set in conformity with said stored measured usage ~~for~~ corresponding to said next set of threads.

16. (Original) The computer program product of Claim 15, wherein said program instructions further comprise program instructions for setting a state of said hardware performance monitor for said

next set of threads in conformity with a result of said retrieving and determining.

17. (Currently Amended) The computer program product of Claim 15, wherein said program instructions for sending comprise program instructions for setting, within said device controller, a threshold level of total usage for said device in conformity with said retrieved previously-stored per-thread measured device usage for said next set of threads, whereby said power management state of said device is set automatically by said device controller in conformity with said set threshold.

18. (Original) The computer program product of Claim 15, wherein said program instructions for first retrieving comprise program instructions for reading collected per-thread counts of accesses to said device from one or more performance monitor units.

19. (Original) The computer program product of Claim 15, wherein said device is a memory module, and wherein said first retrieving retrieves a frequency of accesses to said memory module by each of multiple threads from a performance monitor that measures memory accesses to said module, and wherein said sending send commands to a memory controller that controls a power management state of said memory module.

20. (Original) The computer program product of Claim 15, wherein said device is a memory module, and wherein said first retrieving retrieves a frequency of accesses to said memory module by each of multiple threads from a memory controller that controls access to said memory module, and wherein said sending send commands to said memory controller, whereby said memory controller controls a power management state of said memory module in conformity with a result of said first retrieving.